IC 半导体封装测试流程

第 1 章 前言

1.1 半导体芯片封装的目的

[10, 13]

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-
-
-

1-1 TSOP

Figure 1-1 TSOP Package Cross-section

230

3 50 10% 1K 10K

-40 60

100% 120

MEMS [1]

3D

-
-
-

DRAM/NAND

57nm 1G 2G 45nm

2G SD 45nm

1.4 TSOP 叠层芯片技术研究和重要性和意义

TSOP DRAM TSOP

TinyBGA 50% DDR/DDRRII

TinyBGA NAND

IC Insight 2005 NAND 64%

4% 16 2006 NAND

30% 2006 8% 3

DRAMeXchange 2007 NAND Flash NAND Flash

2007 39 36.8% NAND

NAND TSOP

SiP TSOP

NAND SiP TSOP SiP

SMD SiP TSOP TSOP SMD

SD Mini SD CF MP3/MP4 SDRAM SiP

SiP

SMD PBGA TSOP

TSOP Intel NAND/NOR PBGA

TSOP Intel Micron IMFT(IM Flash Technology)

NAND TSOP iPod NAND

NAND 20% 5

2007 25% NAND

TSOP 55%

TSOP

第 2 章 单芯片 TSOP 封装技术介绍

Front-of-line FOL End-of-line EOL

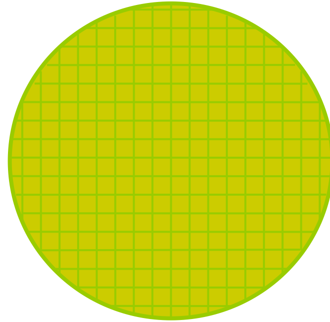
FOL Leadframe Substrate

EOL [7]

2.1 前道生产工艺

1 (wafer)

-3 (Wafer Fab)



2-1

Figure 2-1 Wafer

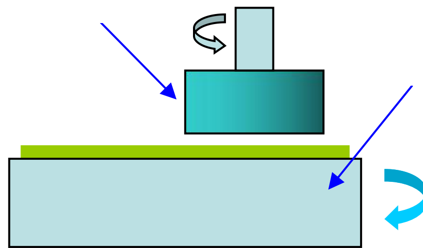
2 (Backgrinding)

0.7mm

-4

TSOP

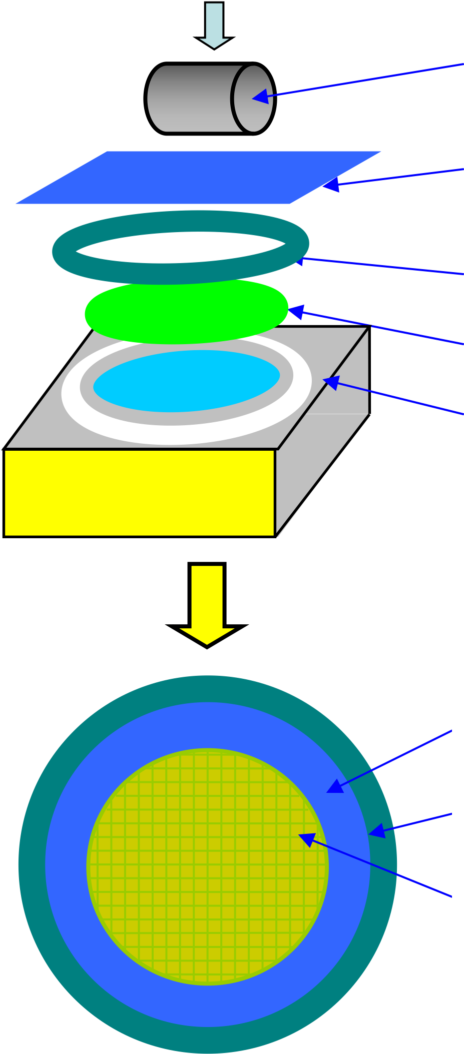
0.28mm



2-2

Figure 2-2 Backgrinding Process

3 (Wafer Mount)



2-3
Figure 2-3 Wafer Mount

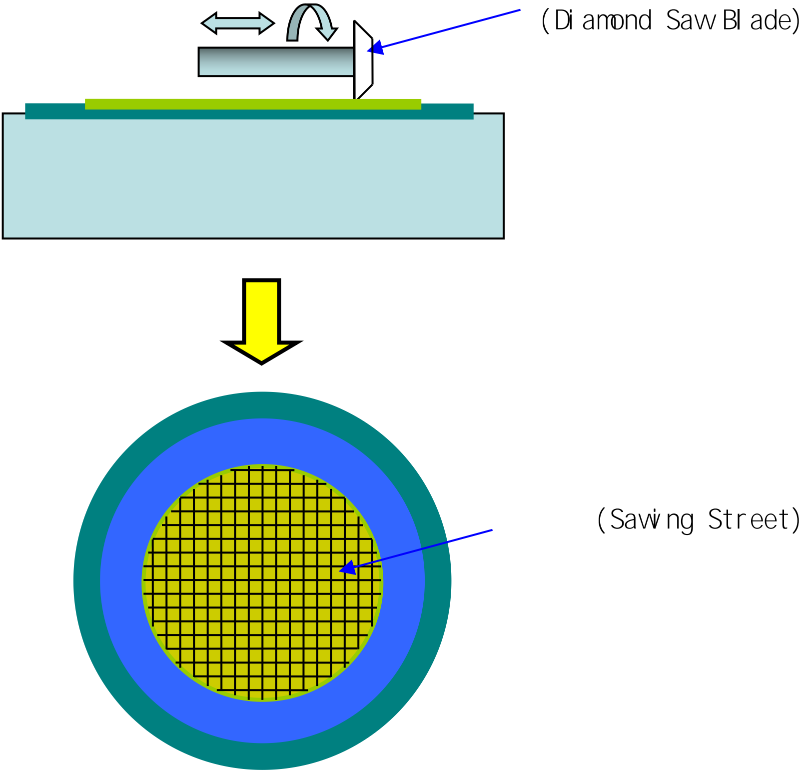
-5

Wafer Ring

(Blue Tape)

-5

4 (Die Sawing)



2-4

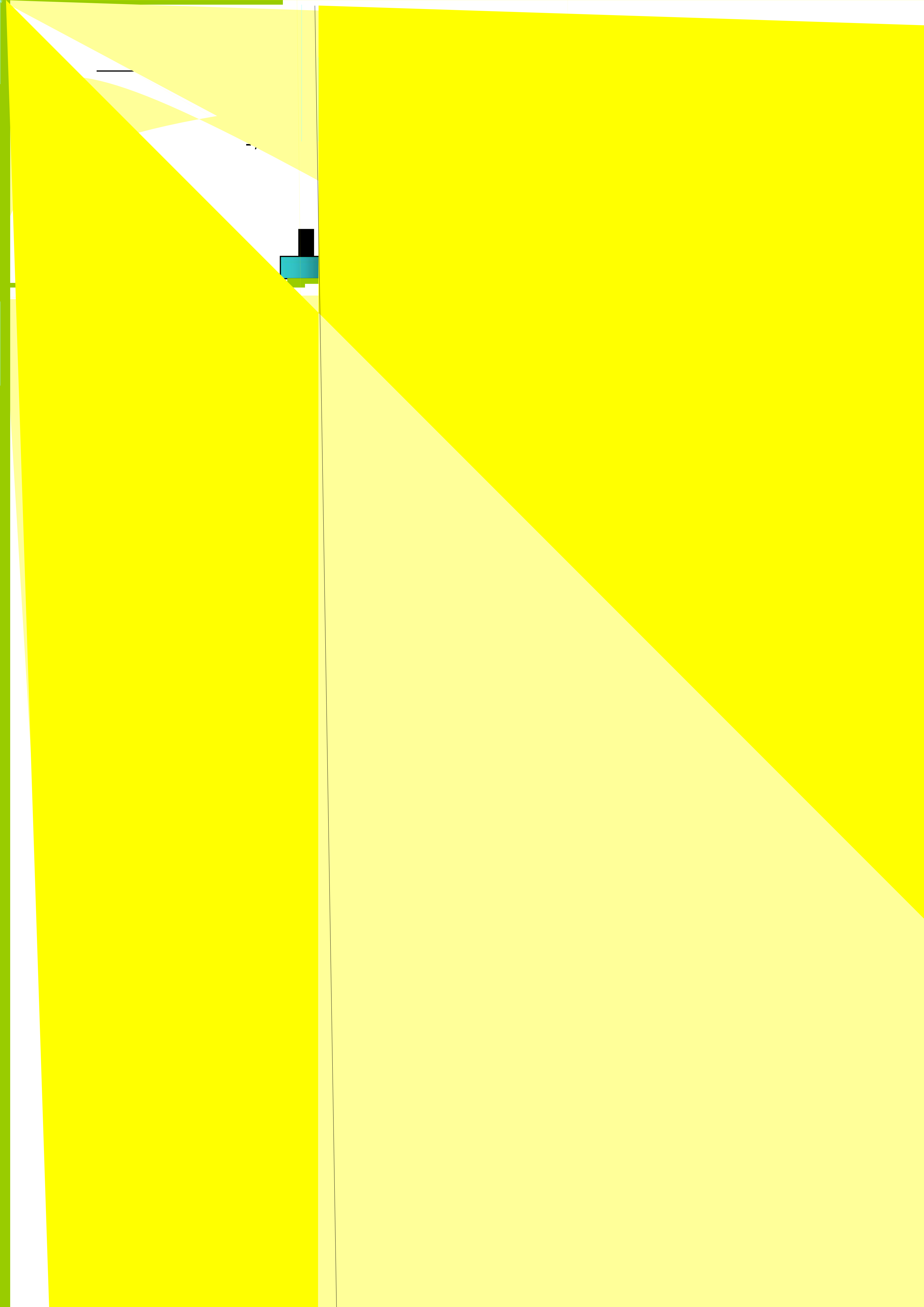
Figure 2-4 Wafer Sawing

-6

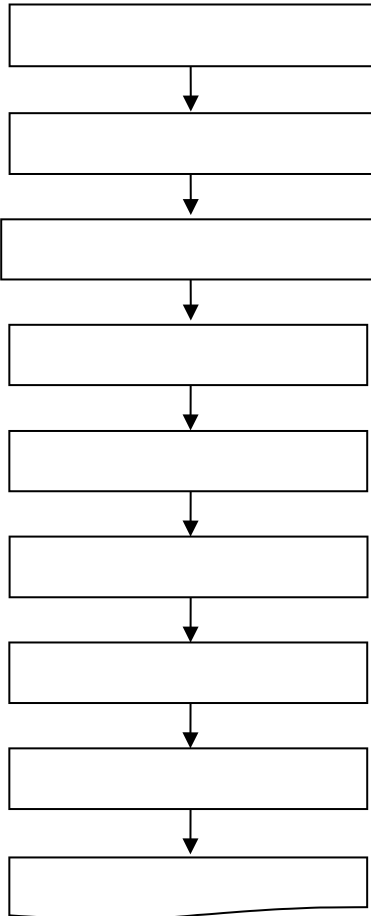
-6

5 (Die Attach)

-7a

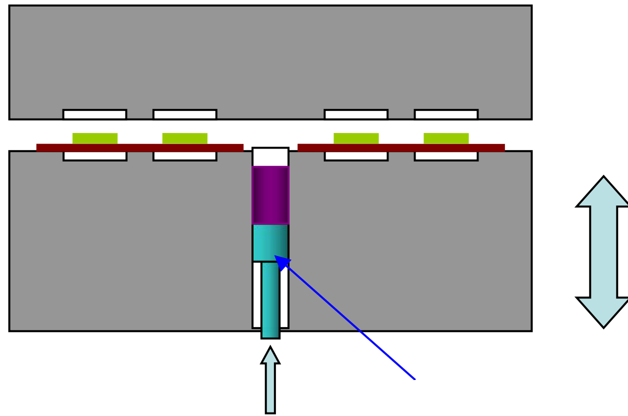


2.2 后道生产工艺：



100%

1 (Molding)



-9b

2 (Trim)

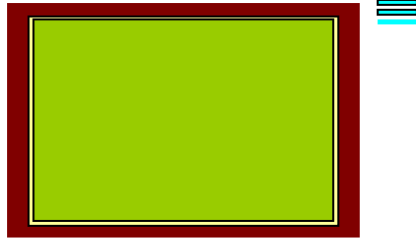
-10 -9b

2-8

Figure 2-8 Trim Process

3 (Plating)

-11 -10



第 3 章 实验环境、设备及材料

23+/-3 50+/10%

-1 -2

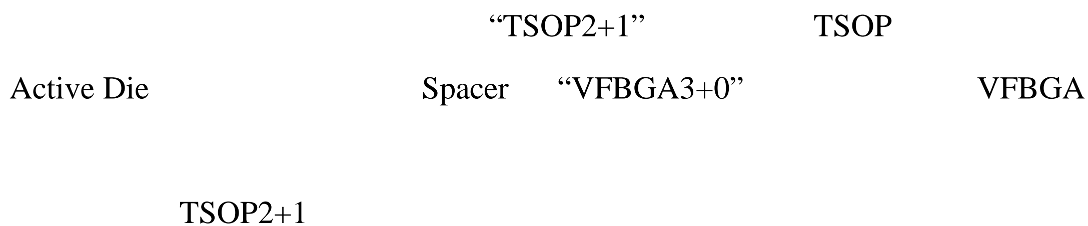
3-1

(B/G)		DISCO DFG-850	TSK PG300
(W/M)		TAKATORI ATM-8100	TSK PG300
(D/S)		DISCO DFD640/651	TSK A-WD-300 DISCO DFD6361 DISCO DFD651
(D/A)		ESEC2007/2008HS	ESEC2008 XP
		ASM AD889	ASM AD8912
		SHINKAWA UTC-250	SHINKAWA UTC1000/2000
(W/B)		K&S 8028	K&S8028 PPS

3-2

(W/M)			Epoxy Film Tape
(D/A)			Epoxy Film
(D/A)			
(W/B)		99.99%	
(MOLD)		EME-G700	EME-G700V
(PLATING)			

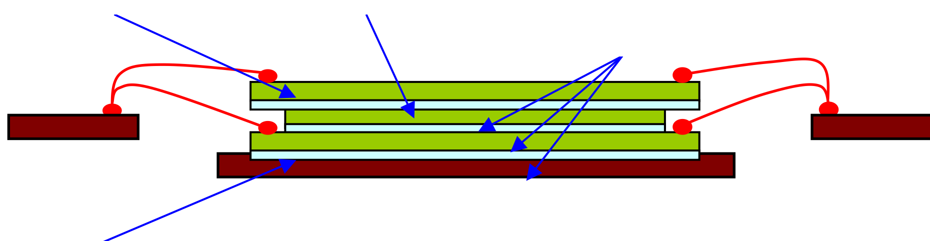
第 4 章 TSOP 叠层芯片封装技术的实现



"TSOP2+1" TSOP

Active Die Spacer "VFBGA3+0" VFBGA

TSOP2+1



4-1 TSOP2+1

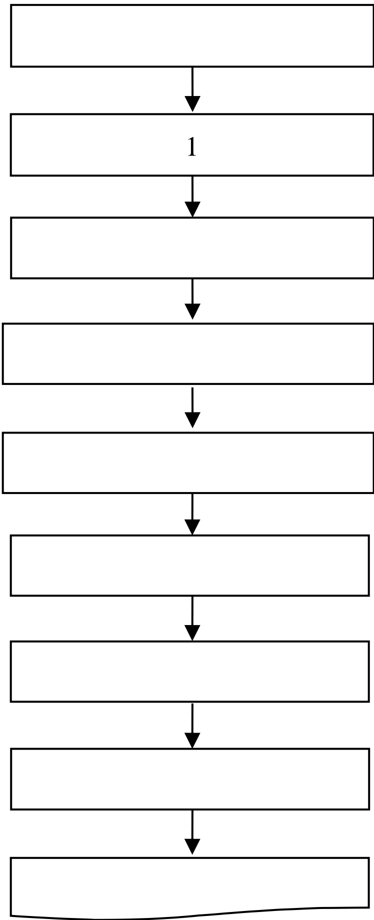
Figure 4-1 TSOP2+1

4.1 三种实现叠层芯片的封装的工艺

TSOP2+X

4.1.1 第一种方法，TSOP2+1，使用多次重复单芯片的工艺

[8]



(D/A)

(W/B) TSOP2+1 (D/A) (W/B)

(Die Crack)

4.2

4.1.2 第二种方法，TSOP2+1，使用环氧树脂薄膜作为芯片贴合剂

4.1.3

4.1.4 三种[illegible]的对比

TSOP2+X

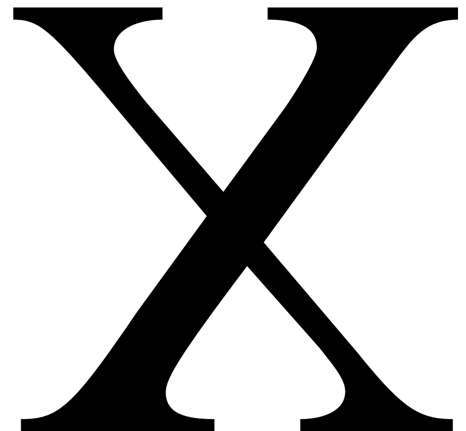
4-1

99.5%

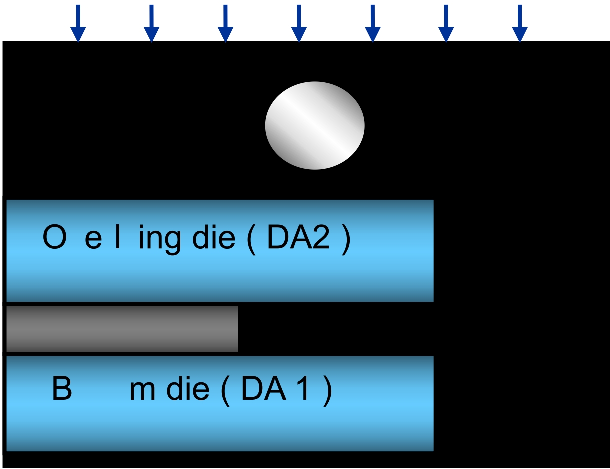
(W/M)

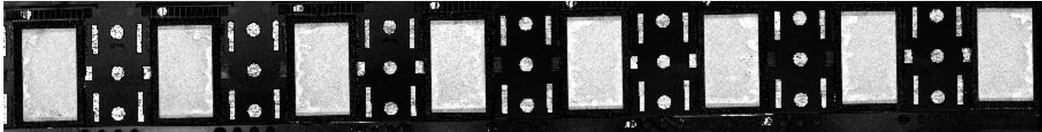
99.8-99.9%

(D/A)



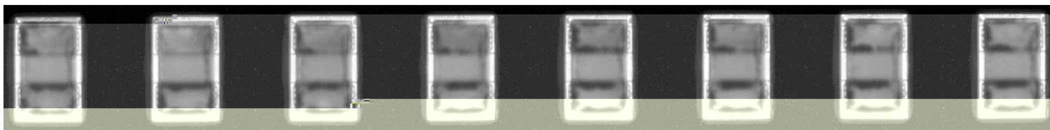
4.2 使用液态环氧树脂银浆作为粘合时的芯片破裂(DD


O e l ing die (DA2)
B m die (DA 1)



4-6

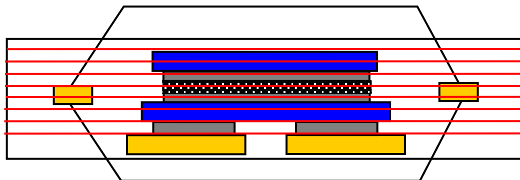
Figure 4-6 C-Scan Photo, Top



4-7

Figure 4-7 Through Scan Photo

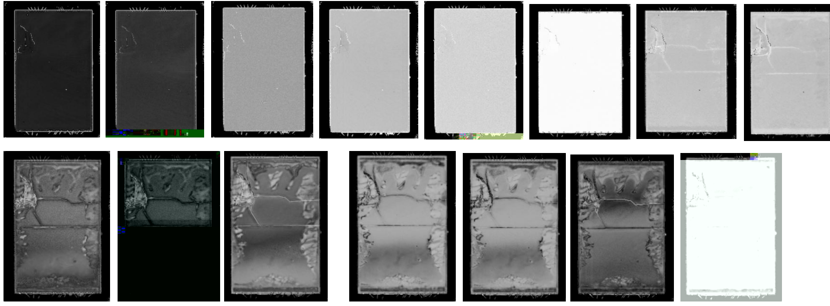
TAMI Tomographic Acoustic Micro Imaging



4-8 TAMI

Figure 4-8 How TAMI works

TAMI



4-9　TAMI

Figure 4-9 Sample photo of TAMI

(Pattern)

95%

“　”

4-10

Figure 4-10 Recommended Epoxy Pattern

95%　(Die Crack)

0

TAMI

95%

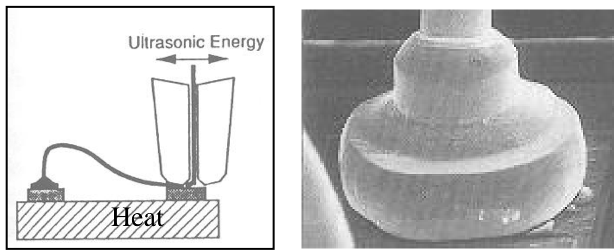
0.1mm　3

(Die Crack)

4.3 叠层芯片封装技术的引线键合的技术

190-210 60KHz 120KHz

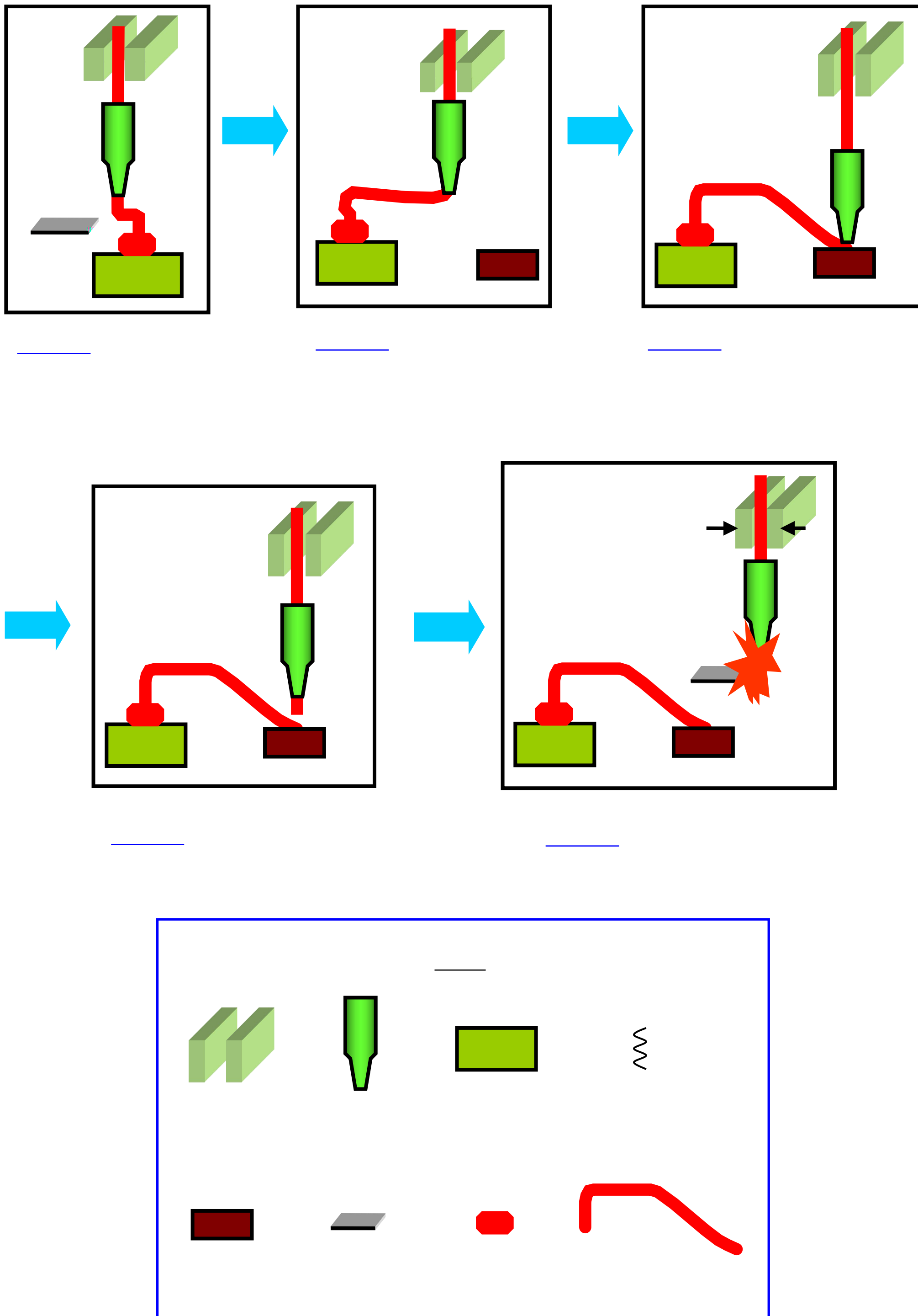
120KHz 0.038mm TSOP 0.025mm 0.020mm



4-11

Figure 4-11 Gold Ball Bond

TSOP



4-13

Figure 4-13 Standard Gold Ball Bond Process

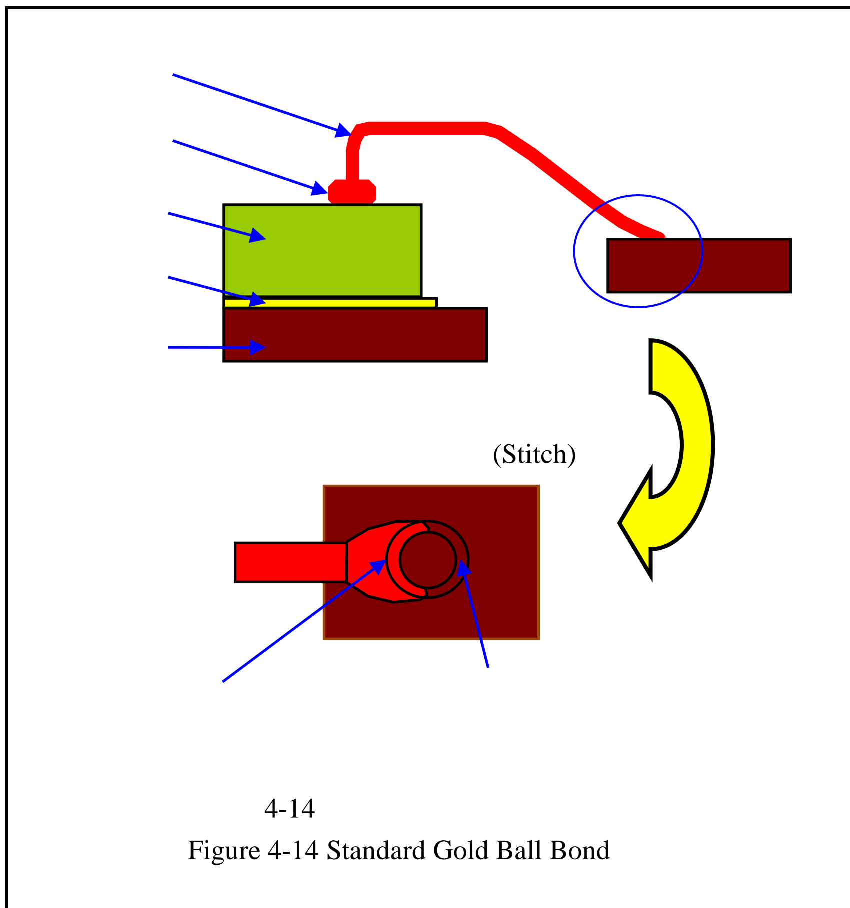
4.3.2 金丝球焊反打方式（SSB）的工艺步骤

SSB Standoff Stitch Bond

SSB Reverse Looping

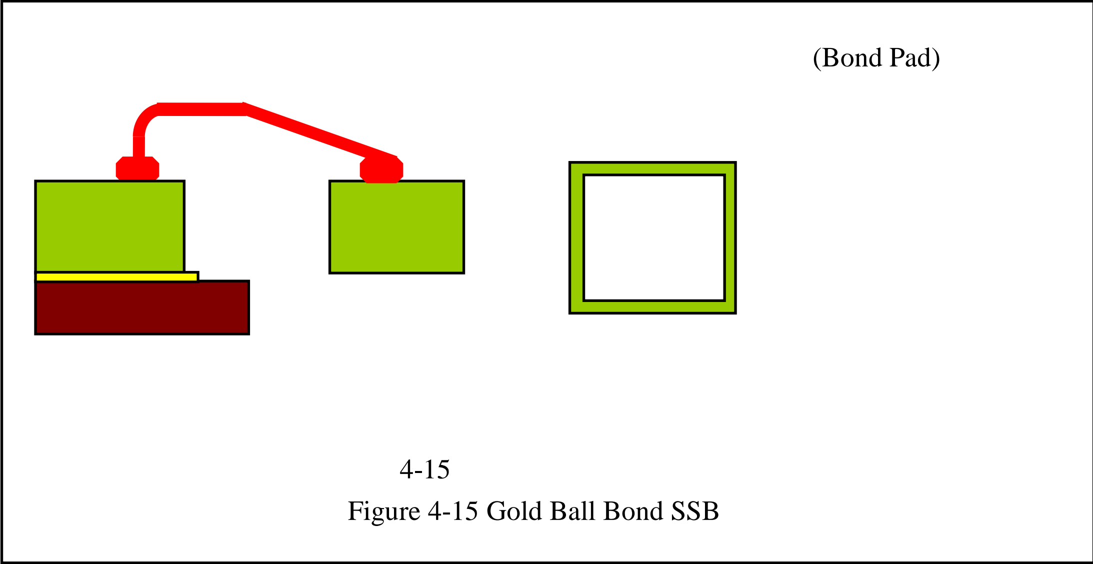
-26 -27

SSB



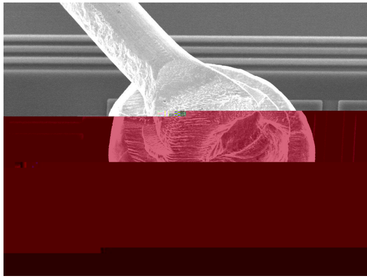
4-14

Figure 4-14 Standard Gold Ball Bond



4-15

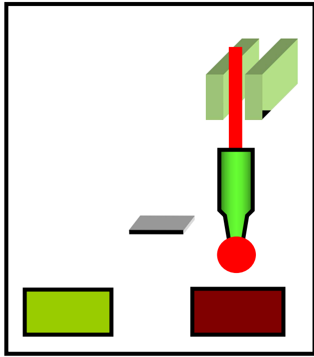
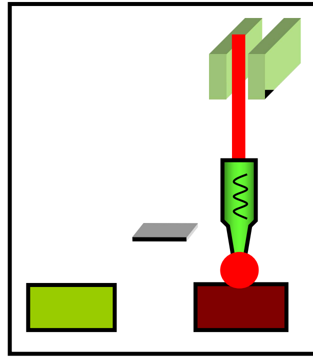
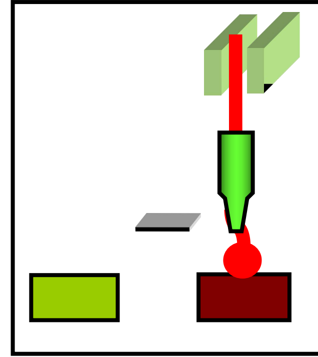
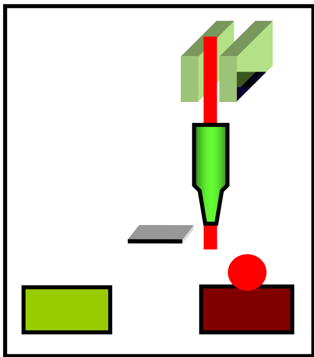
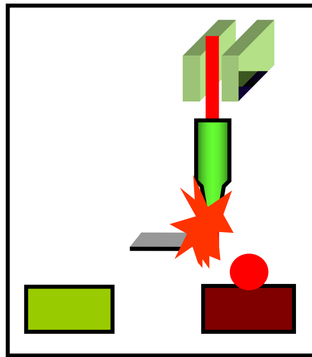
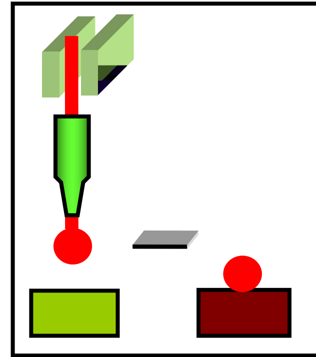
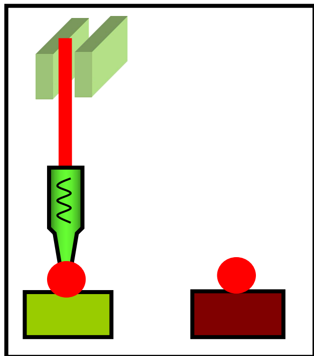
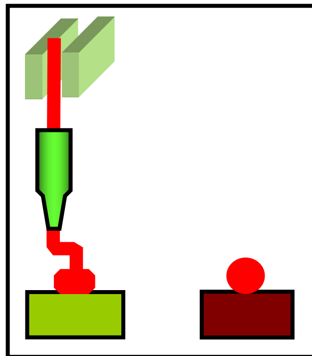
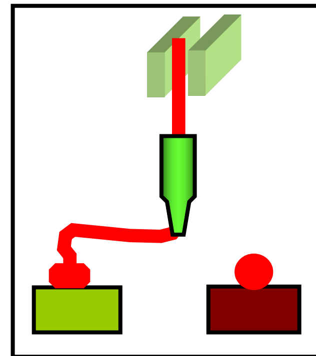
Figure 4-15 Gold Ball Bond SSB

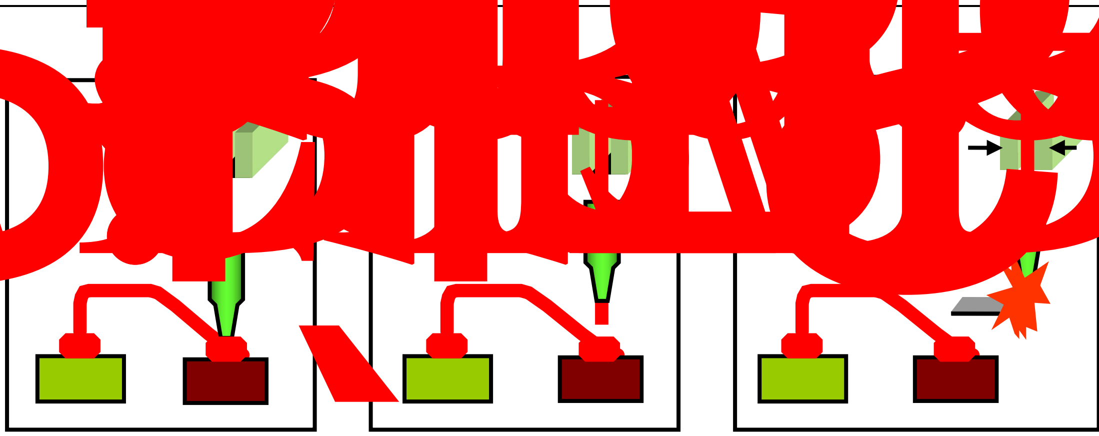


4-16 SEM

Figure 4-16 Gold Ball Bond SSB, Stitch SEM Photo

SSB



4-17
Figure 4-17 Gold Ball Bond SSB Process Steps

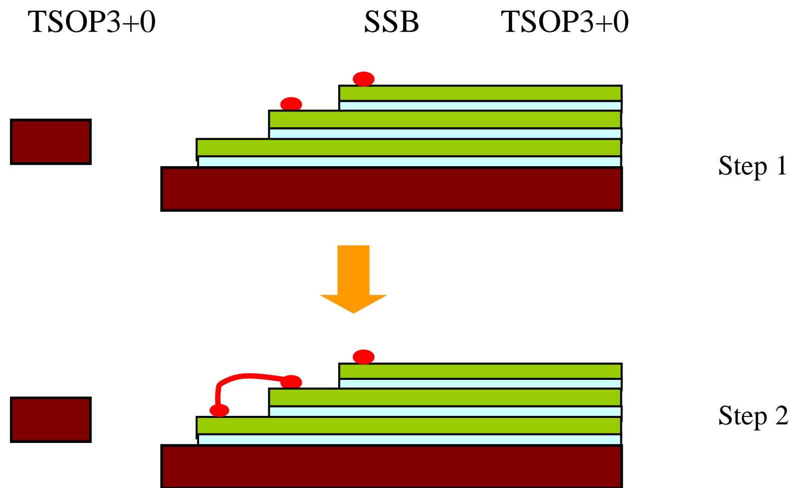
SSB

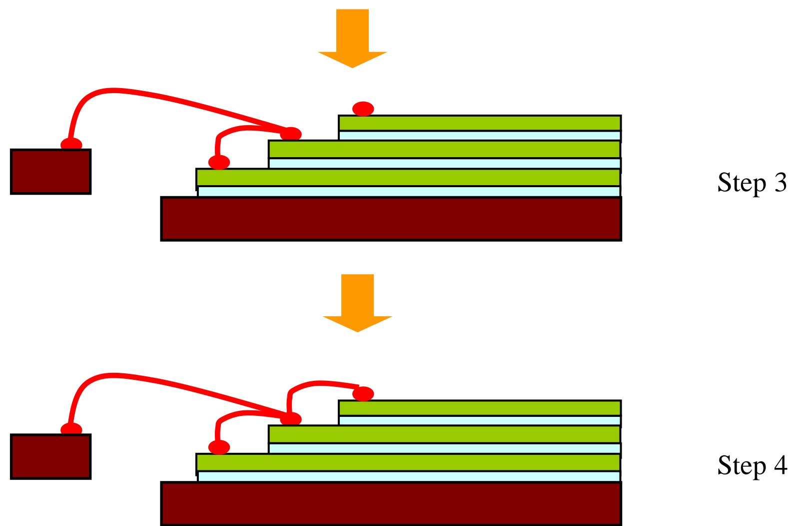
SSB 4 8

SSB

4.3.3 用金丝球焊反打方式（SSB）完成叠层芯片的引线键合

TSOP3+0 SSB TSOP3+0





4-18 TSOP3+0

Figure 4-18(Continue) TSOP3+0 Gold Ball Bond SSB Formation Step

Step 1: Die 2 Die 3 (Bump)

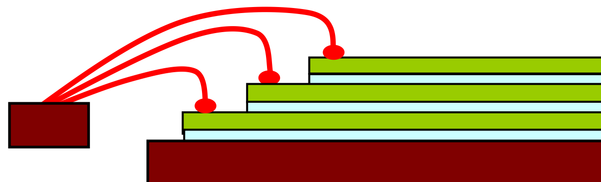
Step 2: SSB Die 1 Die 2

Step 3: SSB Die 2

Step 4: SSB Die 2 Die 3

SSB SSB

4.3.4 金丝球焊正打方式与反打方式（SSB）的对比



4-19 TSOP3+0

Figure 4-19 TSOP3+0 Gold Ball Standard(Forward) Bond

4

4 SSB

SSB -31

TSOP2+1

4.4 单芯片与叠层芯片封装技术的区别

TSOP2+1)

4-20 TSOP2+1

Figure 4-20 TSOP2+1

1.

(D/A) (W/B)

2.

1/2

3. FOL

-1

4. (D/A) (W/B) (D/A) (W/B)

5.

-2

DFG850

300mm 0.15mm

ESEC 2007/2008HS ASM AD889 300mm

ESEC 2008XP ASM AD8912

SSB UTC1000

UTC2000 K&S Maxum Plus K&S Maxum Ultra

TSOP4+0 TSOP5+0 TSOP4+3

SIP 2007

TSOP SIP TSOP SIP

TSOP 55%

TSOP